REMARKS

Claims 11-20 and 22-34 are pending in this application. By this Amendment, Applicants amend the Title of the Invention and Claim 23.

The Title of the Invention was objected to for not being indicative of the claimed invention. Applicants have amended the Title of the Invention to be indicative of the claimed invention. Accordingly, Applicants respectfully request reconsideration and withdrawal of this objection.

Claim 23 was objected to for containing an informality. Applicants have amended claim 23 to correct the informality noted by the Examiner. Accordingly, Applicants respectfully request reconsideration and withdrawal of this objection.

Claims 14, 15 and 23 were rejected to under 35 U.S.C. § 103(a) as being unpatentable over Furuhashi et al. (U.S. 6,011,564) in view of Dye (U.S. 5,664,162). Claims 11-13, 16-20, 22, 24, 26-28, 30-32 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Furuhashi et al. in view of Dye, and further in view of Troeller et al. (U.S. 5,768,445). And claims 19, 25 and 33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Furuhashi et al. in view of Dye and Troeller et al., and further in view of Schilling et al. (U.S. 6,236,405). These rejections are respectfully traversed.

Claim 14 recites:

> "An apparatus for image processing, comprising:
> a processor including a data decompression circuit;
> a first storage device having texture data and electronically coupled to said processor; and
> **a texture buffer having decompressed texture data and electrically coupled to said processor**; wherein
> **transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor.**" (Emphasis added)

Claims 15 and 23 recite features that are similar to the features recited in claim 14, including the emphasized features.

The Examiner acknowledged that Furuhashi et al. fails to teach or suggest a first data bus and a second data bus, wherein the first data bus carries texture data between not claimed.

a texture buffer and a processor faster than the second data bus carries texture data from the storage device and the processor, storing decompressed texture data in a texture buffer, a texture buffer having decompressed texture data and electronically coupled to the processor, wherein transmission of texture data between the texture buffer and the processor is faster than transmission of texture data between the storage device and the processor. However, the Examiner alleged that Dye teaches all of these features in col. 2, lines 53-54, col. 3, lines 17-23, col. 15, lines 23-62, col. 17, line 42 through col. 18, line 6, and col. 19, lines 1-9. Thus, the Examiner concluded that it would have been obvious "to modify the image processing system of Furuhashi et al. by the graphics accelerator means of Dye because both inventions share similar technological environments of decompression/decoding and compression/coding graphics imaging data." Applicants respectfully disagree.

Dye merely teaches that "it is desirable to provide a graphics processor to perform high level graphics functions and to achieve faster graphic data transfer without significantly depreciating the performance of the computer system" (see col. 3, lines 17-23). To accomplish this objective, Dye provides a processor having two separate and independent memory controllers to achieve a dual interface architecture. However, contrary to the Examiner's allegations and the present claimed invention, Dye neither teaches nor suggests an apparatus in which "transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor" as recited in the present claimed invention. In fact, Dye merely discloses that "such operations as texture mapping from u. v space and aligning non-aligned data during data transfer are performed with ease" (see col. 19, lines 1-5). Dye fails to teach or suggest any texture buffer or any specific devices or circuits to perform the transmission of the texture data between a texture buffer and a processor and between a storage device and a processor, and certainly fails to teach or suggest "a texture buffer having decompressed texture data and electrically coupled to said processor" wherein "transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor" as recited in the present claimed invention.

Looks good! 2/5/03

The Issue! 8/14/03

makes the suggestion

Finale!

Rejected

In addition, the Examiner alleged that it would have been obvious "to modify the image processing system of Furuhashi et al. by the graphics accelerator means of Dye because both inventions share similar technological environments of decompression/decoding and compression/coding graphics imaging data." However, the mere fact that Furuhashi et al. and Dye are in "similar technological environments of decompression/decoding and compression/coding graphics imaging data" would not provide sufficient motivation to combine the teachings of Dye with Furuhashi et al. At best, the Examiner's comments regarding obviousness amount to an assertion that one of ordinary skill in the relevant art would have been able to arrive at Applicants' invention because he had the necessary skills to carry out the requisite features of the present invention. This is an inappropriate standard for obviousness. That which is within the capabilities of one skilled in the art is not synonymous with obviousness. See Ex Parte Levengood, 28 USPQ 2d 1300 (Bd. Pat. App. & Inter. 1993). The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Gordon, 221 USPQ 1125 (Fed. Cir. 1984). In this case, there is absolutely no suggest in either prior art reference of the modification necessary to achieve Applicants' claimed invention.

Accordingly, Applicants respectfully submit that Furuhashi et al. and Dye, taken individually or in combination, fail to teach or suggest the unique combination and arrangement of elements recited in claims 14, 15 and 23 of the present application.

In view of the foregoing, Applicant respectfully submits that claims 14, 15 and 23 are allowable. Claims 11-14 and 16-20 and claims 22 and 24-26 are dependent upon claims 14 and 23, respectively, and are therefore allowable for at least the reasons that claims 14 and 23 are allowable.

In view of the foregoing Amendments and Remarks, Applicant respectfully submits that this Application is in condition for allowance. Favorable consideration and prompt allowance are respectfully solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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Attorneys for Applicant

Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

KEATING & BENNETT LLP
10400 Eaton Place, Suite 312
Fairfax, VA 22030
Telephone: (703) 385-5200
Facsimile: (703) 385-5080

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE OF THE INVENTION:

IMAGE PROCESSING [UNIT AND IMAGE PROCESSING METHOD] WHEREIN DECOMPRESSION AND COMPRESSION METHODS PROVIDE FASTER TRANSMISSION OF TEXTURE DATA BETWEEN A TEXTURE BUFFER AND A PROCESSOR THAN BETWEEN A STORAGE DEVICE AND A PROCESSOR

IN THE CLAIMS:

23. An image processing method comprising the steps of:

providing compressed texture data in a storage device;

reading said compressed texture data from said storage device and decompressing said compressed texture data;

storing said decompressed texture data in a texture buffer; and

providing a processor, and transferring data between said texture buffer and said processor faster than transferring data between said storage device and said processor.